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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/935,166	08/21/2001	Jian Zhang	1552-14	9222

996 7590 04/30/2004

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ART UNIT	**PAPER NUMBER**
2133	4

DATE MAILED: 04/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/935,166	ZHANG, JIAN	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-36 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-36 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 August 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3, 8/1/02.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 5-6, 10-12, 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Lahmeyer (US 4,649,541).

Lahmeyer anticipates claim 5.

Lahmeyer teaches a computing system for decoding a Reed-Solomon-encoded string of data, the computing system comprising a processor circuit operable to: receive a first Reed-Solomon code word; receive a second Reed-Solomon code word after receiving the first code word; and while receiving the second code word, decoding the first decoding step of the first code word with a constant or approximately constant level of processing (col. 1, lines 12-15, lines 38-41, lines 51-54 and lines 62-65, Lahmeyer).

- Lahmeyer anticipates claim 6.

Lahmeyer teaches the computing system wherein: receiving the second code word comprises receiving the second code word during a time period having a duration t; and decoding the first code word comprises performing a first decoding step of the first code word during the time period (col. 1, lines 38-41, lines 51-54 and lines 62-65, Lahmeyer).

- Lahmeyer anticipates claim 10.

Lahmeyer teaches a computing system for decoding a Reed-Solomon-encoded string of data (col. 1, lines 12-15, Lahmeyer) the computing system comprising a processor circuit operable to (col. 1, lines 38-41, Lahmeyer): 1. receive the Reed-Solomon-encoded string of data in t seconds; 2. calculate a syndrome in said t seconds; 3. calculate the coefficients of an error locator polynomial in said t seconds;

4. determine the roots of an error locator polynomial in said t seconds; and 5. determine the magnitude of an error and correcting the error in said t seconds (col. 2, lines 3-37, Lahmeyer).

- Lahmeyer anticipates claim 11.

Lahmeyer teaches the computing system wherein said Reed-Solomon-encoded string of data comprises: a first number of data symbols each including second number of bits; and a third number of parity symbols each including the second number of bits (col. 2, lines 7-11, Lahmeyer).

- Lahmeyer anticipates claim 12.

Lahmeyer teaches the computing system wherein said Reed-Solomon-encoded string of data comprises: a first number of symbol blocks each including a second number of symbols; a third number of parity symbols; and wherein the third number is an integer multiple of the first number (col. 3, lines 43-47, lines 57-60, col. 4, lines 28-30, Lahmeyer).

- Lahmeyer anticipates claim 14.

Lahmeyer teaches the computing system wherein the processor circuit executes a Chien Search to determine the roots of the error locator polynomial (col. 8, lines 3-5, Lahmeyer).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) in view of Shao et al. (US 4,868,828).

As per claim 1, Lahmeyer teaches a computing system for decoding a Reed-Solomon-encoded string of data, the computing system comprising a processor circuit operable to: receive a Reed-Solomon code word; and decode the code word with a constant or approximately constant level of processing (col. 1, lines 12-15, lines 38-41, lines 51-54 and lines 62-65, Lahmeyer).

However Lahmeyer does not explicitly teach the specific use of decoding the code word in software.

Shao et al. in an analogous art teach that the advantage of this new algorithm over previous methods discussed by I. S. Reed, T. K. Truong and R. L. Miller, "Decoding of B.C.H. and RS codes with errors and erasures using continued fractions," Electronic Letters, vol. 15, no. 17, Aug. 16, 1976, pp. 542-544, is that separate computations of the errata locator polynomial and the errata evaluator polynomial usually needed can be avoided. This new decoding algorithm is highly suitable for both VLSI and software implementation (col. 4, lines 67-68, col. 5, lines 1-8, Shao et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Shao et al. by including an additional step of decoding the code word in software.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that decoding the code word in software would provide the opportunity to reduce hardware requirements, reduce maintenance requirements for the decoder and provide faster processing.

6. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) and Shao et al. (US 4,868,828) as applied to claim 1 above, and further in view of Deodhar (US 4,567,594).

As per claim 2, Lahmeyer and Shao et al. substantially teach the claim 1 (as rejected above).

However Lahmeyer and Shao et al. do not explicitly teach the specific use of the computing system wherein: receiving the code word comprises receiving the code word in a time having a duration t; and

decoding the code word comprises decoding the code word in a number of steps each having a duration of t.

Deodhar in an analogous art teaches that the invention divides the Reed-Solomon decoding process into a sequence of well-defined steps requiring a minimum of inter-step parameter transfers. These steps are implemented in the preferred embodiment by a plurality of processors, one for each of the defined steps, operating in a pipelined manner so as to provide efficient and fast decoding (col. 2, lines 8-15, Deodhar).

Deodhar teaches that the machine implemented method is performed in a manner such that the code words of a sector read from said disk are decoded over a plurality of consecutive time periods, wherein the step of determining partial syndromes is such that during a first time period partial syndromes are determined for all of the code words of the sector, wherein the step of determining an error location polynomial is such that during a next following second time period error location polynomials are determined for all of the code words of the sector (col. 16, lines 19-29, Deodhar).

Deodhar also teaches that a first processor is operative during each time period for receiving a new sector of data read from said disk and responsive thereto for producing partial syndrome signals representative of the partial syndromes of all of the code words of the corresponding sector. A second processor is operative during each time period and responsive to partial syndrome signals produced by said first processor one time period earlier for producing error location polynomial signals representative of the error location polynomial of the code words of the corresponding sector (col. 17, lines 46-57, Deodhar).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Deodhar by including an additional step of using the computing system wherein: receiving the code word comprises receiving the code word in a time having a duration t; and decoding the code word comprises decoding the code word in a number of steps each having a duration of t.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity

to reduce time delay for decoding the code words and the processing load on the decoder is evenly distributed at all times.

- As per claim 3, Lahmeyer, Shao et al. and Deodhar teach the additional limitations. Deodhar teaches that receiving the code word comprises receiving the code word in a time having a duration t; and decoding the code word comprises decoding the code word in a number of sequential steps each having a duration of t (figure 5, col. 2, lines 8-15, col. 16, lines 19-29, col. 17, lines 46-57, Deodhar).

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) and Shao et al. (US 4,868,828) as applied to claim 1 above, and further in view of Iwasaki et al. (US 4,677,623).

As per claim 4, Lahmeyer and Shao et al. substantially teach the claim 1 (as rejected above). However Lahmeyer and Shao et al. do not explicitly teach the specific use of the system wherein: the code word comprises a number n of equal-length blocks; receiving the code word comprises receiving each of the blocks in a time having a duration t/n; and decoding the code word comprises decoding the code word in a number of sequential steps each having n sub steps of a duration t/n.

Iwasaki et al. in an analogous art teach that the code word F(x) of the cyclic code is divided into the number of blocks equal to the number of bits of the period e.sub.n of the polynomial P.sub.n (x), (col. 6, lines 20-23, Iwasaki et al.).

Iwasaki et al. teach the decoding operation. The decoding is done by the following three steps.

(S1) Generation of syndromes S.sub.c (x), S.sub.p1 (x), S.sub.p2 (x) and

S.sub.p3 (x)

(S2) Preshifting of FSRC, FSRP.sub.1, FSRP.sub.2 and FSRP.sub.3

(S3) Determination of error pattern B(x) and error location j

A circuit shown in FIG. 2 controls the above three steps, and FIGS. 3, 4 and 5 show timing charts for the processes in the steps (S1), (S2) and (S3), respectively. The signal lines 161-164 are rendered high level in synchronism with the first bit data of the input data 160. As shown in FIG. 3, when the syndromes

S.sub.c (x), S.sub.p1 (x), S.sub.p2 (x) and S.sub.p3 (x) are generated, the signal lines 161-164 are rendered high level only for the period of data input.

(col. 7, lines 62-68, col. 8, lines 1-3. lines 24-26, lines 32-34, Iwasaki et al.).

Iwasaki et al. also teach the final step (S3). This step determines the error pattern B(x) and the error location j.As shown in FIG. 6, the signal lines 161-164 are rendered high level at the clock .phi..sub.2 following to the error detection start signal 217 to start the shiftings in the FSRC, FSRP.sub.1, FSRP.sub.2 and FSRP.sub.3, and the output 214 of the counter 213 is incremented from "0" (col. 10, lines 10-11, lines 19-23, Iwasaki et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Iwasaki et al. by including an additional step of using the system wherein: the code word comprises a number n of equal-length blocks; receiving the code word comprises receiving each of the blocks in a time having a duration t/n; and decoding the code word comprises decoding the code word in a number of sequential steps each having n sub steps of a duration t/n.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce the time delay for decoding, spread the decoding processing load on the processors evenly and minimize system failure.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) as applied to claim 5 above, and further in view of Deodhar (US 4,567,594).

As per claim 7, Lahmeyer substantially teach the claimed invention described in claim 5 (as rejected above).

However Lahmeyer does not explicitly teach the specific use of the computing system wherein receiving the second code word comprises receiving the second code word during a first time period having a duration t; wherein decoding the first code word comprises performing a first decoding step on the first code word during the first time period; receiving a third code word during a second time period having the

duration t; performing a second decoding step on the first code word during the second time period; and performing the first decoding step on the second code word during the second time period.

Deodhar in an analogous art teaches a disk having data recorded in a track, said track being divided into a plurality of sectors, said data being recorded in each sector as a plurality of interleaved code words along with check data having values determined in accordance with Reed-Solomon decoding principles; means for sequentially reading sectors of data from said disk; and processing means to which sectors of data read from said disk are sequentially applied, said processing means being operative to detect and correct errors in sectors of data read from said disk by performing a plurality of consecutive processing operations thereon in accordance with said Reed-Solomon decoding principles; said processing means comprising a plurality of processors, one for each of said consecutive processing operations, said processors operating in a pipelined manner and at a rate with respect to sequentially read sectors so as to provide for essentially real-time correction of data errors in sectors read from said disk (col. 16, lines 61-68, col. 17, lines 1-14, Deodhar).

Deodhar also teaches the invention, wherein said processing means operates over successive time periods, wherein said processing means includes a buffer for temporarily storing sectors of data applied to said processing means, and wherein said plurality of processors includes:

a first processor operative during each time period for receiving a new sector of data read from said disk and responsive thereto for producing partial syndrome signals representative of the partial syndromes of all of the code words of the corresponding sector;

a second processor operative during each time period and responsive to partial syndrome signals produced by said first processor one time period earlier for producing error location polynomial signals representative of the error location polynomial of the code words of the corresponding sector;

a third processor operative during each time period and responsive to error location polynomial signals produced by said second processor one time period earlier for producing error location signals representative of the locations of data errors in at least one of the code words of the corresponding sector;

said third processor also being operative during each time period in response to error location signals produced by said second processor two time periods earlier for producing error location signals corresponding to the locations of data errors for those code words of the corresponding sector for which error location signals were not produced by said third processor in the preceding time period (col. 17, lines 40-57, col. 18, lines 1-14, Deodhar).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Deodhar by including an additional step of using the computing system wherein receiving the second code word comprises receiving the second code word during a first time period having a duration t; wherein decoding the first code word comprises performing a first decoding step on the first code word during the first time period; receiving a third code word during a second time period having the duration t; performing a second decoding step on the first code word during the second time period; and performing the first decoding step on the second code word during the second time period.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to spread the decoding processing load on the processors evenly by decoding one code word while receiving the next code word and minimize system failure.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) as applied to claim 5 above, and further in view of Iwasaki et al. (US 4,677,623).

As per claim 8, Lahmeyer substantially teach the claimed invention described in claim 5 (as rejected above).

However Lahmeyer does not explicitly teach the specific use of the computing system wherein: the first and second code words each comprise a number n of equal-length blocks; receiving the first and second code words comprises receiving each of the blocks in n sequential time periods each having a duration t/n; and decoding the first code word comprises decoding the first code word in n sequential sub steps each having a duration t/n.

Iwasaki et al. in an analogous art teach that the code word F(x) of the cyclic code is divided into the number of blocks equal to the number of bits of the period e.sub.n of the polynomial P.sub.n (x), (col. 6, lines 20-23, Iwasaki et al.).

Iwasaki et al. teach the decoding operation. The decoding is done by the following three steps.

(S1) Generation of syndromes S.sub.c (x), S.sub.p1 (x), S.sub.p2 (x) and

S.sub.p3 (x)

(S2) Preshifting of FSRC, FSRP.sub.1, FSRP.sub.2 and FSRP.sub.3

(S3) Determination of error pattern B(x) and error location j

A circuit shown in FIG. 2 controls the above three steps, and FIGS. 3, 4 and 5 show timing charts for the processes in the steps (S1), (S2) and (S3), respectively. The signal lines 161-164 are rendered high level in synchronism with the first bit data of the input data 160. As shown in FIG. 3, when the syndromes S.sub.c (x), S.sub.p1 (x), S.sub.p2 (x) and S.sub.p3 (x) are generated, the signal lines 161-164 are rendered high level only for the period of data input.

(col. 7, lines 62-68, col. 8, lines 1-3. lines 24-26, lines 32-34, Iwasaki et al.).

Iwasaki et al. also teach the final step (S3). This step determines the error pattern B(x) and the error location j.As shown in FIG. 6, the signal lines 161-164 are rendered high level at the clock .phi..sub.2 following to the error detection start signal 217 to start the shiftings in the FSRC, FSRP.sub.1, FSRP.sub.2 and FSRP.sub.3, and the output 214 of the counter 213 is incremented from "0" (col. 10, lines 10-11, lines 19-23, Iwasaki et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Iwasaki et al. by including an additional step of using the system wherein: the first and second code words each comprise a number n of equal-length blocks; receiving the first and second code words comprises receiving each of the blocks in n sequential time periods each having a duration t/n; and decoding the first code word comprises decoding the first code word in n sequential sub steps each having a duration t/n.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity

to reduce the time delay for decoding, spread the decoding processing load on the processors evenly and minimize system failure.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) in view of Deodhar (US 4,567,594) and Iwasaki et al. (US 4,677,623).

As per claim 9, Lahmeyer teaches a computing system for decoding a Reed-Solomon-encoded string of data, the computing system comprising a processor circuit (col. 1, lines 12-15, lines 38-41, Lahmeyer). However Lahmeyer does not explicitly teach the specific use of each code word comprising a number n of equal-length blocks.

Iwasaki et al. in an analogous art teach that the code word F(x) of the cyclic code is divided into the number of blocks equal to the number of bits of the period e.sub.n of the polynomial P.sub.n (x), (col. 6, lines 20-23, Iwasaki et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Iwasaki et al. by including an additional step of using a code word comprising a number n of equal-length blocks.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to make the time interval to decode one block of code word equal to time interval to receive one block of next code word and reduce delay to decode a code word.

Lahmeyer also does not explicitly teach the specific use of receiving five Reed-Solomon code words, each during a time period having a duration t, while receiving the second code word, decoding the first step of the first code word in n sequential sub steps each having a duration t/n; while receiving the third code word, decoding the second step of the first code word in n sequential sub steps each having a duration t/n and decoding the first step of the second code word in n sequential sub steps each having a duration t/n; while receiving the fourth code word, decoding the third step of the first code word in n sequential sub steps each having a duration t/n and decoding the second step of the second code word in n sequential sub steps each having a duration t/n and decoding the first step of the third code word in n sequential sub steps each having a duration t/n; and while receiving the fifth code word, decoding the

fourth step of the first code word in n sequential sub steps each having a duration t/n and decoding the third step of the second code word in n sequential sub steps each having a duration t/n and decoding the second step of the third code word in n sequential sub steps each having a duration t/n and decoding the first step of the fourth code word in n sequential sub steps each having a duration t/n.

However Deodhar in an analogous art teaches a disk having data recorded in a track, said track being divided into a plurality of sectors, said data being recorded in each sector as a plurality of interleaved code words along with check data having values determined in accordance with Reed-Solomon decoding principles; means for sequentially reading sectors of data from said disk; and processing means to which sectors of data read from said disk are sequentially applied, said processing means being operative to detect and correct errors in sectors of data read from said disk by performing a plurality of consecutive processing operations thereon in accordance with said Reed-Solomon decoding principles; said processing means comprising a plurality of processors, one for each of said consecutive processing operations, said processors operating in a pipelined manner and at a rate with respect to sequentially read sectors so as to provide for essentially real-time correction of data errors in sectors read from said disk (col. 16, lines 61-68, col. 17, lines 1-14, Deodhar).

Deodhar also teaches the invention, wherein said processing means operates over successive time periods, wherein said processing means includes a buffer for temporarily storing sectors of data applied to said processing means, and wherein said plurality of processors includes:

a first processor operative during each time period for receiving a new sector of data read from said disk and responsive thereto for producing partial syndrome signals representative of the partial syndromes of all of the code words of the corresponding sector;

a second processor operative during each time period and responsive to partial syndrome signals produced by said first processor one time period earlier for producing error location polynomial signals representative of the error location polynomial of the code words of the corresponding sector;

a third processor operative during each time period and responsive to error location polynomial signals produced by said second processor one time period earlier for producing error location signals

representative of the locations of data errors in at least one of the code words of the corresponding sector;

said third processor also being operative during each time period in response to error location signals produced by said second processor two time periods earlier for producing error location signals corresponding to the locations of data errors for those code words of the corresponding sector for which error location signals were not produced by said third processor in the preceding time period (col. 17, lines 40-57, col. 18, lines 1-14, Deodhar).

Deodhar teaches a fourth processor operative during each time period and responsive to error location signals produced by said third processor one time period earlier for producing error value signals representative of the error values in at least one of the code words of the corresponding sector; said fourth processor also being operative during each time period in response to error location signals produced by said third processor two time periods earlier for producing error value signals representative of code words of the corresponding sector for which error value signals were not produced by said fourth processor in the preceding time period; and

a fifth processor operative during each time period for receiving a different sector of data from said buffer and for correcting errors in the code words of a different sector in response to corresponding error location signals and error value signals produced by said third and fourth processors during previous time periods (col. 18, lines 15-35, Deodhar).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Deodhar by including an additional step of receiving five Reed-Solomon code words, each during a time period having a duration t, while receiving the second code word, decoding the first step of the first code word in n sequential sub steps each having a duration t/n; while receiving the third code word, decoding the second step of the first code word in n sequential sub steps each having a duration t/n and decoding the first step of the second code word in n sequential sub steps each having a duration t/n; while receiving the fourth code word, decoding the third step of the first code word in n sequential sub steps each having a duration t/n and decoding the second step of the second code word in n sequential sub steps each having a duration t/n and decoding the first

step of the third code word in n sequential sub steps each having a duration t/n; and while receiving the fifth code word, decoding the fourth step of the first code word in n sequential sub steps each having a duration t/n and decoding the third step of the second code word in n sequential sub steps each having a duration t/n and decoding the second step of the third code word in n sequential sub steps each having a duration t/n and decoding the first step of the fourth code word in n sequential sub steps each having a duration t/n.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to spread the decoding processing load on the processors evenly by decoding one code word while receiving the next code word and minimize system failure.

11. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) as applied to claim 10 above, and further in view of Oh et al. (US 5,583,499).

As per claim 13, Lahmeyer substantially teaches the claimed invention described in claim 10 (as rejected above).

However Lahmeyer does not explicitly teach the specific use of the computing system wherein the processor circuit executes a Berlekamp-Massey Algorithm to calculate the coefficients of the error locator polynomial.

Oh et al. in an analogous art teach that a popular algorithm for obtaining the coefficients of the error locator polynomial is the Berlekamp-Massey algorithm (col. 2, lines 8-10, Oh et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Oh et al. by including an additional step of using the computing system wherein the processor circuit executes a Berlekamp-Massey Algorithm to calculate the coefficients of the error locator polynomial.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to provide apparatus for implementing Galois field arithmetic using fewer components, fewer data paths and higher speed than a general purpose digital computer employed for this purpose.

12. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) as applied to claim 10 above, and further in view of Sammartino et al. (US 6,511,280 B1).

As per claim 15, Lahmeyer substantially teaches the claimed invention described in claim 10 (as rejected above).

However Lahmeyer does not explicitly teach the specific use of the computing system wherein the processor circuit executes a Forney Algorithm to determine the magnitude of the errors in the received digital code word.

Sammartino et al. in an analogous art teach finding the roots of the ti(x) to determine the error locations, and determining the magnitude of the errors and erasures by applying a modified version of the Forney algorithm (col. 6, lines 37-40, Sammartino et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Sammartino et al. by including an additional step of using the computing system wherein the processor circuit executes a Forney Algorithm to determine the magnitude of the errors in the received digital code word.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to use concatenated coding for implementing a code with a very long block length and a large error-correcting capability.

13. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) as applied to claim 10 above, and further in view of Iwasaki et al. (US 4,677,623).

As per claim 16, Lahmeyer substantially teaches the claimed invention described in claim 10 (as rejected above). Lahmeyer also teaches a first number of symbol blocks each including a second number of symbols; a third number of parity symbols; and wherein the third number is an integer multiple of the first number (col. 3, lines 43-47, lines 57-60, col. 4, lines 28-30, Lahmeyer).

However Lahmeyer does not explicitly teach specifically that the processor circuit is operable to divide each of the tasks (a)-(e) into the first number of subtasks, the processor operable to execute each of the

subtasks in a time equal to t divided by the first number such that the processor load is even for every symbol block.

Iwasaki et al. in an analogous art teach that the code word F(x) of the cyclic code is divided into the number of blocks equal to the number of bits of the period e.sub.n of the polynomial P.sub.n (x), (col. 6, lines 20-23, Iwasaki et al.).

Iwasaki et al. teach the decoding operation. The decoding is done by the following three steps.

(S1) Generation of syndromes S.sub.c (x), S.sub.p1 (x), S.sub.p2 (x) and

S.sub.p3 (x)

(S2) Preshifting of FSRC, FSRP.sub.1, FSRP.sub.2 and FSRP.sub.3

(S3) Determination of error pattern B(x) and error location j

A circuit shown in FIG. 2 controls the above three steps, and FIGS. 3, 4 and 5 show timing charts for the processes in the steps (S1), (S2) and (S3), respectively. The signal lines 161-164 are rendered high level in synchronism with the first bit data of the input data 160. As shown in FIG. 3, when the syndromes S.sub.c (x), S.sub.p1 (x), S.sub.p2 (x) and S.sub.p3 (x) are generated, the signal lines 161-164 are rendered high level only for the period of data input.

(col. 7, lines 62-68, col. 8, lines 1-3. lines 24-26, lines 32-34, Iwasaki et al.).

Iwasaki et al. also teach the final step (S3). This step determines the error pattern B(x) and the error location j.As shown in FIG. 6, the signal lines 161-164 are rendered high level at the clock .phi..sub.2 following to the error detection start signal 217 to start the shiftings in the FSRC, FSRP.sub.1, FSRP.sub.2 and FSRP.sub.3, and the output 214 of the counter 213 is incremented from "0" (col. 10, lines 10-11, lines 19-23, Iwasaki et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Iwasaki et al. by including additionally that the processor circuit is operable to divide each of the tasks (a)-(e) into the first number of subtasks, the processor operable to execute each of the subtasks in a time equal to t divided by the first number such that the processor load is even for every symbol block.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce the time delay for decoding, spread the decoding processing load on the processors evenly and minimize system failure.

14. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) as applied to claim 10 above, and further in view of Deodhar (US 4,567,594).

As per claim 17, Lahmeyer substantially teaches the claimed invention described in claim 10 (as rejected above). Lahmeyer also teaches a first number of symbol blocks each including a second number of symbols; a third number of parity symbols; and wherein the third number is an integer multiple of the first number (col. 3, lines 43-47, lines 57-60, col. 4, lines 28-30, Lahmeyer).

However Lahmeyer does not explicitly teach specifically that the processor circuit is operable to divide each of the tasks (a)-(e) into the first number of subtasks, the processor circuit operable to pipeline the tasks (a)-(e) by simultaneously executing one subtask from each task in a time equal to t divided by the first number such that the processor-circuit load is even for every symbol block.

Deodhar in an analogous art teaches that the invention divides the Reed-Solomon decoding process into a sequence of well-defined steps requiring a minimum of inter-step parameter transfers. These steps are implemented in the preferred embodiment by a plurality of processors, one for each of the defined steps, operating in a pipelined manner so as to provide efficient and fast decoding (col. 2, lines 8-15, Deodhar).

Deodhar teaches that the machine implemented method is performed in a manner such that the code words of a sector read from said disk are decoded over a plurality of consecutive time periods, wherein the step of determining partial syndromes is such that during a first time period partial syndromes are determined for all of the code words of the sector, wherein the step of determining an error location polynomial is such that during a next following second time period error location polynomials are determined for all of the code words of the sector (col. 16, lines 19-29, Deodhar).

Deodhar also teaches that a first processor is operative during each time period for receiving a new sector of data read from said disk and responsive thereto for producing partial syndrome signals representative of the partial syndromes of all of the code words of the corresponding sector. A second

processor is operative during each time period and responsive to partial syndrome signals produced by said first processor one time period earlier for producing error location polynomial signals representative of the error location polynomial of the code words of the corresponding sector (col. 17, lines 46-57, Deodhar).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Deodhar by including an additional step of using the processor circuit operable to divide each of the tasks (a)-(e) into the first number of subtasks, the processor circuit operable to pipeline the tasks (a)-(e) by simultaneously executing one subtask from each task in a time equal to t divided by the first number such that the processor-circuit load is even for every symbol block.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce time delay for decoding the code words and the processing load on the decoder is evenly distributed at all times.

15. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lahmeyer (US 4,649,541) as applied to claim 10 above, and further in view of Deodhar (US 4,567,594).

As per claim 18, Lahmeyer substantially teaches the claimed invention described in claim 10 (as rejected above). Lahmeyer also teaches a first number of symbol blocks each including a second number of symbols; a third number of parity symbols; and wherein the third number is an integer multiple of the first number (col. 3, lines 43-47, lines 57-60, col. 4, lines 28-30, Lahmeyer).

However Lahmeyer does not explicitly teach the specific use of the computing system, wherein: the processor circuit comprises multiple processors; said Reed-Solomon-encoded string of data comprises: a first number of symbol blocks each including a second number of symbols; a third number of parity symbols; and wherein the third number is an integer multiple of the first number; and the processor circuit is operable to divide each of the tasks (a)-(e) into the first number of subtasks, the processor circuit operable to pipeline the tasks (a)-(e) by simultaneously executing one subtask from each task with a respective processor.

Deodhar in an analogous art teaches that the invention divides the Reed-Solomon decoding process into a sequence of well-defined steps requiring a minimum of inter-step parameter transfers. These steps are implemented in the preferred embodiment by a plurality of processors, one for each of the defined steps, operating in a pipelined manner so as to provide efficient and fast decoding (col. 2, lines 8-15, Deodhar). Deodhar teaches that the machine implemented method is performed in a manner such that the code words of a sector read from said disk are decoded over a plurality of consecutive time periods, wherein the step of determining partial syndromes is such that during a first time period partial syndromes are determined for all of the code words of the sector, wherein the step of determining an error location polynomial is such that during a next following second time period error location polynomials are determined for all of the code words of the sector (col. 16, lines 19-29, Deodhar).

Deodhar also teaches that a first processor is operative during each time period for receiving a new sector of data read from said disk and responsive thereto for producing partial syndrome signals representative of the partial syndromes of all of the code words of the corresponding sector. A second processor is operative during each time period and responsive to partial syndrome signals produced by said first processor one time period earlier for producing error location polynomial signals representative of the error location polynomial of the code words of the corresponding sector (figure 5, col. 17, lines 46-57, Deodhar).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lahmeyer's patent with the teachings of Deodhar by including an additional step of using the computing system, wherein: the processor circuit comprises multiple processors; said Reed-Solomon-encoded string of data comprises: a first number of symbol blocks each including a second number of symbols; a third number of parity symbols; and wherein the third number is an integer multiple of the first number; and the processor circuit is operable to divide each of the tasks (a)-(e) into the first number of subtasks, the processor circuit operable to pipeline the tasks (a)-(e) by simultaneously executing one subtask from each task with a respective processor.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity

to reduce time delay for decoding the code words and the processing load on the decoder is evenly distributed at all times.

16. Claim 19 follows the same limitations as claim 1. See rejection to claim 1, above. Claim 19 is rejected under the same rational as to claim 1 rejected above.

17. Claim 20 follows the same limitations as claim 2. See rejection to claim 2, above. Claim 20 is rejected under the same rational as to claim 2 rejected above.

18. Claim 21 follows the same limitations as claim 3. See rejection to claim 3, above. Claim 21 is rejected under the same rational as to claim 3 rejected above.

19. Claim 22 follows the same limitations as claim 4. See rejection to claim 4, above. Claim 22 is rejected under the same rational as to claim 4 rejected above.

20. Claim 23 follows the same limitations as claim 5. See rejection to claim 5, above. Claim 23 is rejected under the same rational as to claim 5 rejected above.

21. Claim 24 follows the same limitations as claim 6. See rejection to claim 6, above. Claim 24 is rejected under the same rational as to claim 6 rejected above.

22. Claim 25 follows the same limitations as claim 7. See rejection to claim 7, above. Claim 25 is rejected under the same rational as to claim 7 rejected above.

23. Claim 26 follows the same limitations as claim 8. See rejection to claim 8, above. Claim 26 is rejected under the same rational as to claim 8 rejected above.

24. Claim 27 follows the same limitations as claim 9. See rejection to claim 9, above. Claim 27 is rejected under the same rational as to claim 9 rejected above.

25. Claim 28 follows the same limitations as claim 10. See rejection to claim 10, above. Claim 28 is rejected under the same rational as to claim 10 rejected above.

26. Claim 29 follows the same limitations as claim 11. See rejection to claim 11, above. Claim 29 is rejected under the same rational as to claim 11 rejected above.

27. Claim 30 follows the same limitations as claim 12. See rejection to claim 12, above. Claim 30 is rejected under the same rational as to claim 12 rejected above.

28. Claim 31 follows the same limitations as claim 13. See rejection to claim 13, above. Claim 31 is rejected under the same rational as to claim 13 rejected above.

29. Claim 32 follows the same limitations as claim 14. See rejection to claim 14, above. Claim 32 is rejected under the same rational as to claim 14 rejected above.

30. Claim 33 follows the same limitations as claim 15. See rejection to claim 15, above. Claim 33 is rejected under the same rational as to claim 15 rejected above.

31. Claim 34 follows the same limitations as claim 16. See rejection to claim 16, above. Claim 34 is rejected under the same rational as to claim 16 rejected above.

32. Claim 35 follows the same limitations as claim 17. See rejection to claim 17, above. Claim 35 is rejected under the same rational as to claim 17 rejected above.

33. Claim 36 follows the same limitations as claim 18. See rejection to claim 18, above. Claim 36 is rejected under the same rational as to claim 18 rejected above.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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